canceled claim 1. Applicants respectfully submit that the modifications to the claims provided herein are supported by the originally filed specification.

The rejection of claims 1-4, 7, and 8 under 35 U.S.C. §103(a) as being unpatentable over Shimbo et al. (U.S. Patent No. 4,738,935) in view of Lee et al. (U.S. Patent No. 4,900,372) and Narayan et al. (U.S. Patent No. 5,208,182) is hereby traversed and reconsideration thereof is respectfully requested in view of Amendments to the claims contained herein and the following remarks.

Independent claim 21, which replaces canceled claim 1, is directed to a method for forming low defect density epitaxial layers on lattice-mismatched substrates. The method includes the steps of (a) bonding a first substrate layer having a first lattice constant and a first thermal expansion coefficient to a second substrate layer having a second lattice constant and a second thermal expansion coefficient, thereby forming a composite substrate having a composite lattice constant and a composite thermal expansion coefficient; (b) disposing a buffer layer on the composite substrate, the buffer layer having a buffer layer lattice constant and a buffer layer thermal expansion coefficient; and (c) disposing a first epilayer on the buffer layer, the first epilayer having a first epilayer lattice constant and a first epilayer thermal expansion coefficient.

The second lattice constant and second thermal expansion coefficient of the second substrate layer is selected so that if the first epilayer lattice constant is greater than the composite lattice constant, then the first epilayer thermal expansion coefficient is smaller than the composite thermal expansion coefficient; and if the first epilayer lattice constant is smaller than the composite lattice constant, then the first epilayer thermal expansion coefficient is greater than the composite thermal expansion coefficient.

The buffer layer lattice constant is selected to be substantially identical to the epilayer lattice constant and the buffer layer thermal expansion coefficient is selected so that if the buffer layer lattice constant is greater than the composite lattice constant, then the buffer layer thermal expansion coefficient is greater than the composite thermal expansion coefficient, and if the buffer layer lattice constant is smaller than the composite

lattice constant, then the buffer layer thermal expansion coefficient is smaller than the composite thermal expansion coefficient.

Claims 2-11, 18, and 19 depend from claim 21.

The Shimbo reference ('935) discloses a method of manufacturing a compound semiconductor device wherein two compound semiconductor substrates having given impurity concentrations and thicknesses are bonded, thereby forming a junction with good electrical characteristics, irrespective of lattice constant mismatch therebetween. As illustrated in the Figures and described in cols. 2 and 3, the surface of each of two compound semiconductor substrates is mirror-polished; the mirror-polished surfaces of the two compound semiconductor substrates are brought in contact with each other in a clean atmosphere and in a state wherein substantially no foreign substances are present therebetween; and the compound semiconductor substrates which are in contact with each other are annealed so as to provide a bonded structure. Shimbo mentions combinations of different types of semiconductor substrates, such as GaAs/InP, ZnS/GaAs, InP/InSb, GaP/InP and CdS/InP. The stated object of Shimbo's approach is to form a junction with good electrical characteristics, as described with particularity with reference to the Examples 1-5. Shimbo is only concerned with the mismatch between the lattice constants and the thermal expansion coefficients as to their effect on the electrical interface properties between the two compound semiconductor substrates. Unlike the subject matter disclosed in the present invention, however, Shimbo does not disclose, teach or suggest that the composite lattice constant and the composite thermal expansion coefficient of a composite substrate formed from the two compound semiconductor substrates are of significance for the devices proposed in the '935 patent. Neither does Shimbo disclose the use of the so formed device as a composite substrate for further device fabrication.

The Lee reference ('372) discloses a method for producing wafers having deposited layers of III-V materials on Si or Ge/Si or other single crystal substrates. Lee discloses various annealing methods to minimize the defects and balance the stresses. Furthermore, defects near the III-V/substrate interface region can be decreased further by doping or diffusing certain impurities into the III-V layer prior to annealing. Also, by

incorporating steps both in-situ and ex-situ the growth chamber, improvements in the final layered substrate are observed. Lee is only concerned with the thermal strain layer and, unlike the subject matter disclosed in the present invention, does not suggest adapting and/or modifying the single crystal substrates for producing wafers having a decreased incidence of defects and a balanced thermal strain.

The Narayan reference ('182) discloses a method of forming a gallium arsenide on silicon heterostructure which includes the use of strained layer superlattices in combination with rapid thermal annealing to achieve a reduced threading dislocation density in the epilayers. The GaAs/Si structure shown in Fig. 4 of Narayan and indicated by the reference numerals 10, 12 is not a composite substrate with the characteristic features disclosed in the present invention. Moreover, although Narayan mentions that threading dislocations and other defects in GaAs/Si heterostructures are primarily caused by lattice mismatch between the GaAs and Si layers (a_{Si} =5.43 Å, a_{GaAs} =5.65 Å) and thermal mismatch (coefficient of thermal expansion $_{Si}$ =2.6x10^{-6} K^{-1}, $_{GaAs}$ =5.8x10^{-6} K^{-1}), Narayan does not disclose, teach or suggest replacing the offending Si substrate with a composite substrate having a suitable composite lattice constant and a composite thermal expansion coefficient, as recited in new claim 21 of the present application.

The subject matter of the present application, as recited in claim 21, discloses a particular and novel relationship between the lattice constants and thermal expansion coefficients of the composite substrate, the buffer layer, and the first epitaxial layer for overcoming the generation and propagation of dislocations. The argument that it would have been obvious to combine the Shimbo, Lee and Narayan references to arrive at the subject matter disclosed by Applicants is impermissible hindsight, since a person skilled in the art would not be motivated to use Narayan's structure for further device fabrication, nor would that person be motivated to look for a composite substrate based on the Lee and Narayan references. Moreover, even if these references were known to such person, undue experimentation would be required to arrive at the selection of parameters recited in claim 21. Accordingly, Applicants respectfully submit that the subject matter disclosed in the present invention is non-obvious over the prior art of record and request that the rejection of claim 21 be withdrawn. Claims 2-11 and 18 and 19 should be patentable for the same reason that claim 21 is patentable.

Based on the above Amendment and Remarks, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-832-1000 (direct dial: 617-832-1753).

Respectfully submitted,

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